CLEAN VERSION OF AMENDMENTS

In the Claims:

Please replace claims 9, 17, and 18 with the following amended versions of claims 9, 17, and 18, respectively, cancel claim 14 without prejudice..

C1

9. (Twice amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors.

C2

17. (Amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1 x 10^{11} atoms/cm^2 to about 1 x 10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 1 x 10^{14} atoms/cm^2 to about 1 x 10^{16} atoms/cm^2 at an energy from about 60 keV to about 100 keV.

18. (Amended) A method of forming non-volatile semiconductor memory device, comprising:

providing a semiconductor substrate having a core region comprising memory cells and a peripheral region, wherein word lines in the core region connecting the memory cells are spaced apart by about 1 μm or less;

forming one or more insulating layers for one or more electrostatic discharge protection transistors and one or more other transistors in the peripheral region;

forming a poly layer over the insulating layers;

patterning electrostatic discharge protection transistors and other transistors from the insulating layers and the poly layer;

lightly doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic, boron, and phosphorus at about 1 x 10^{11} atoms/cm^2 to about 1 x 10^{14} atoms/cm^2 at an energy from about 20 keV to about 80 keV;

depositing spacer material over the electrostatic discharge protection transistors and the other transistors;

etching the spacer material to form spacers; and

with the spacers in place, masking the core region and heavily doping source and drain regions for the electrostatic discharge protection transistors with one of arsenic and phosphorus at about 5 x 10^{14} atoms/cm^2 to about 7 x 10^{15} atoms/cm^2 at an energy from about 60 keV to about 100 keV.